

PATENT
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IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant: Ren Uchida Conf.: 9224
Appl. No.: 09/941,683 Group: 2829
Filed: August 30, 2001 Examiner: Patel, Paresh H.
For: TESTING METHOD AND TESTING DEVICE FOR
SEMICONDUCTOR INTEGRATED CIRCUITS

REPLY UNDER 37 C.F.R. § 1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

August 22, 2003

Sir:

In reply to the Office Action dated May 27, 2003, the following amendments and remarks are respectfully submitted in connection with the above-identified application.

This reply includes:

Amendments to the Claims are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks being on page 5 of this paper.

Conclusion beings on page 7 of this paper.